

IN THE CLAIMS

1-11 (Canceled)

12. (Original) A method of forming a via plug, the method comprising:

directing an aerosol stream of particles of a first conductive material onto a sidewall of a via disposed in a substrate or in a dielectric layer disposed on a base layer of an integrated circuit device to form a seed layer of the first conductive material on the sidewall; and

plating the seed layer with a second conductive material.

13. (Original) The method of claim 12, wherein plating the seed layer with a second conductive material comprises plating the seed layer with a second conductive material that is substantially the same as the first conductive material.

14. (Original) The method of claim 12, wherein plating the seed layer with the second conductive material comprises electroplating or electrolessly plating the seed layer with the second conductive material.

15. (Original) The method of claim 12, further comprising before plating the seed layer, aggregating the particles of the first conductive material to form a coherent mass of the first conductive material on the sidewall.

16. (Original) The method of claim 12, wherein the first conductive material is silver and the second conductive material is copper.

17-21 (Canceled)

22. (Original) A method of forming an integrated circuit device, the method comprising:

forming a dielectric layer on a base layer of the integrated circuit device;

forming a via in the dielectric layer terminating at the base layer; and

forming a via plug within the via, wherein forming the via plug comprises:

directing an aerosol stream of particles of a first conductive material onto a

sidewall of the via to form a seed layer of the first conductive material on
the sidewall; and

plating the seed layer with a second conductive material.

23. (Original) The method of claim 22, further comprising before plating the seed layer,

aggregating the particles of the first conductive material to form a coherent mass of the
first conductive material on the sidewall.

24. (Original) The method of claim 22, wherein plating the seed layer with a second conductive

material comprises plating the seed layer with a second conductive material that is
substantially the same as the first conductive material.

25. (Original) The method of claim 22, further comprising forming a metal layer on the

dielectric layer in contact with the via plug so that the via plug interconnects the metal
layer and the base layer.

26-29 (Canceled)

30. (Currently amended) A method of manufacturing an integrated memory circuit, wherein

the memory circuit comprises an array of memory cells connected to column and row
address decoders and a sensing circuit, the method comprising:

forming a via plug in the memory circuit, wherein forming the via plug comprises:

directing an aerosol stream of particles of a first conductive material onto a

sidewall of a via of the memory circuit to deposit the conductive material

within the via to form a seed layer of the first conductive material on the sidewall; and

plating the seed layer with a second conductive material.

31. (Original) The method of claim 30, further comprising before plating the seed layer, aggregating the particles of the first conductive material to form a coherent mass of the first conductive material on the sidewall.
32. (Original) The method of claim 30, wherein plating the seed layer with a second conductive material comprises plating the seed layer with a second conductive material that is substantially the same as the first conductive material.
33. (Original) The method of claim 30, further comprising, before forming the via plug: forming a dielectric layer on a base layer of the memory circuit; and forming the via in the dielectric layer.
34. (Original) The method of claim 33, further comprising forming a metal layer on the dielectric layer in contact with the via plug so that the via plug interconnects the metal layer and the base layer.
35. (New) The method of claim 12, wherein the base layer is a metal layer or an active area of the integrated circuit device.
36. (New) A method of forming a via plug, the method comprising:
forming a through-hole via that passes completely through a substrate or blind-hole via that terminates at a base layer of an integrated circuit device;
directing an aerosol stream of particles of a first conductive material onto a sidewall of the through-hole via or the blind-hole via to form a seed layer of the first conductive material on the sidewall; and

plating the seed layer with a second conductive material.

37. (New) A method of forming a via plug, the method comprising:
- forming a through-hole via that passes completely through a substrate;
 - covering a first end of the via;
 - directing an aerosol stream of particles of a first conductive material through a second end of the via opposite the first end onto a sidewall of the via to form a seed layer of the first conductive material on the sidewall; and
 - plating the seed layer with a second conductive material.
38. (New) The method of claim 37, further comprising uncovering the first end of the via after plating the seed layer with the second conductive material.
39. (New) A method of forming an integrated circuit device, the method comprising:
- forming a dielectric layer on a base layer of the integrated circuit device;
 - forming a through-hole via that passes completely through the dielectric layer and the base layer;
 - covering a first end of the via;
 - forming a via plug within the via, wherein forming the via plug comprises:
 - directing an aerosol stream of particles of a first conductive material through a second end of the via opposite the first end onto a sidewall of the via to form a seed layer of the first conductive material on the sidewall; and
 - plating the seed layer with a second conductive material.
40. (New) The method of claim 39, further comprising uncovering the first end of the via after plating the seed layer with the second conductive material.